REMARKS

The Office Action dated July 27, 2005, has been received and carefully considered. In this response, claims 1, 4-15, and 18 have been amended. Entry of the amendments to claims 1, 4-15, and 18 is respectfully requested. Reconsideration of the outstanding rejections in the present application is also respectfully requested based on the following remarks.

I. THE STATUTORY DOUBLE-PATENTING REJECTION OF CLAIMS 1-17

On page 3 of the Office Action, claims 1-17 were rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-17 of U.S. Patent No. 6,775,328. This rejection is hereby respectfully traversed with partial amendment.

Claim 1 of the present application differs in scope from claim 1 of U.S. Patent No. 6,775,328 in that claim 1 of the present application, as presently set forth, does not require a media driver connectable to a transmission medium. Accordingly, it is respectfully submitted that claim 1 of the present application, as presently set forth, does not claim the same invention as claim 1 of U.S. Patent No. 6,775,328.

Claims 2-9 of the present application are dependent upon claim 1 of the present application. Thus, claims 2-9 of the present application incorporate all limitations and the

corresponding scope of claim 1 of the present application. Accordingly, since, as discussed above, claim 1 of the present application differs in scope from claim 1 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 2-9 of the present application do not claim the same invention as claims 2-9 of U.S. Patent No. 6,775,328.

Claim 10 of the present application differs in scope from claim 10 of U.S. Patent No. 6,775,328 in that claim 10 of the present application, as presently set forth, does not require an internal circuit and a slave circuit connected to the internal circuit. Accordingly, it is respectfully submitted that claim 10 of the present application, as presently set forth, does not claim the same invention as claim 10 of U.S. Patent No. 6,775,328.

Claims 11-14 of the present application are dependent upon claim 10 of the present application. Thus, claims 11-14 of the present application incorporate all limitations and the corresponding scope of claim 10 of the present application. Accordingly, since, as discussed above, claim 10 of the present application differs in scope from claim 10 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 11-14 of the present application do not claim the same invention as claims 11-14 of U.S. Patent No. 6,775,328.

Claim 15 of the present application differs in scope from claim 15 of U.S. Patent No. 6,775,328 in that claim 15 of the present application, as presently set forth, does not require a media driver connectable to a transmission medium. Accordingly, it is respectfully submitted that claim 15 of the present application, as presently set forth, does not claim the same invention as claim 15 of U.S. Patent No. 6,775,328.

Claims 16 and 17 of the present application are dependent upon claim 15 of the present application. Thus, claims 16 and 17 of the present application incorporate all limitations and the corresponding scope of claim 15 of the present application. Accordingly, since, as discussed above, claim 15 of the present application differs in scope from claim 15 of U.S. Patent No. 6,775,328, it is respectfully submitted that claims 16 and 17 of the present application do not claim the same invention as claims 16 and 17 of U.S. Patent No. 6,775,328.

In view of the foregoing, it is respectfully requested that the aforementioned statutory double-patenting rejection of claims 1-17 be withdrawn.

II. THE NON-STATUTORY DOUBLE-PATENTING REJECTION OF CLAIMS 18 AND 19

On page 3 of the Office Action, claims 18 and 19 were rejected under the judicially created doctrine of obviousness-

type double patenting as being unpatentable over claims 18 and 19 of U.S. Patent No. 6,775,328.

A terminal disclaimer is submitted herewith to overcome the non-statutory double patenting rejection of claims 18 and 19.

In view of the foregoing, it is respectfully requested that the aforementioned non-statutory double-patenting rejection of claims 18 and 19 be withdrawn.

III. THE NON-STATUTORY DOUBLE-PATENTING REJECTION OF CLAIM 20

On page 4 of the Office Action, claim 20 was rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 20 of U.S. Patent No. 6,775,328.

A terminal disclaimer is submitted herewith to overcome the non-statutory double patenting rejection of claim 20.

In view of the foregoing, it is respectfully requested that the aforementioned non-statutory double-patenting rejection of claim 20 be withdrawn.

IV. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The

Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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Date: October 27, 2005

APPENDIX A

1 (Currently Amended). A communication device comprising:

a physical layer device having:

~~a media driver connectable to a transmission medium;~~

a media receiver connectable to ~~the~~ a transmission medium;

a serializer/deserializer (serdes) connected to the ~~media driver and the~~ media receiver; and

a master circuit connected to the serdes, the master circuit having:

a first physical layer data driver, the first physical layer data driver driving a first differential signal; and

a first physical layer data receiver; and

a processing circuit having:

an internal circuit; and

a slave circuit connected to the internal circuit and the master circuit, the slave circuit having:

a first processing data receiver connected to the first physical layer data driver, the first processing data receiver outputting a first signal in response to receiving the first differential signal output from the first physical layer data driver; and

a first processing data driver connected to the first physical layer data receiver, and connectable to the first processing data receiver.

2 (Previously Presented). The device of Claim 1,

wherein the master circuit further includes a clock driver connected to the serdes, the clock driver driving a second differential signal;

wherein the slave circuit further includes a clock receiver connected to the clock driver, the clock receiver outputting a clock signal in response to a signal received from the clock driver; and

wherein the first processing data driver is connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver, the first physical layer data receiver receiving the clock signal when the first processing data driver is connected to receive the clock signal, and the first signal when the first processing data driver is connected to receive the first signal.

3 (Original). The device of claim 2 wherein the master circuit further comprises an aligner connected to the first physical layer data receiver, the aligner receiving the clock signal when

the first physical layer data receiver receives the clock signal, the aligner receiving the first signal when the first physical layer data receiver receives the first signal, the aligner having phase comparison circuitry that compares a phase of the clock signal received by the aligner with a phase of the first signal received by the aligner to determine a phase difference.

4 (Currently Amended). The device of claim 3 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signal to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the first differential signal output from the first physical layer data driver so that the first signal received by the aligner is substantially in phase with the clock signal received by the aligner.

5 (Currently Amended). The device of claim 4 wherein the slave circuit further includes:

a first multiplexer connected to the clock ~~input~~ receiver and the first processing data receiver, the first multiplexer passing the clock signal output by the clock receiver when a

first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexer connected to the first multiplexer and the first ~~communication~~ processing data driver, the second multiplexer passing a signal output from the first multiplexer when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexer being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

6 (Currently Amended). The device of claim 5 wherein the slave circuit further includes a serial-to-parallel shift register connected to the clock receiver, the first processing data receiver, and the internal circuit, the clock signal output by the clock receiver clocking the serial-to-parallel shift register.

7 (Currently Amended). The device of claim 5 wherein the slave circuit further includes a parallel-to-serial shift register connected to the internal circuit, the second multiplexer, and

the clock receiver, the parallel-to-serial shift register outputting a data output signal in response to a parallel data signal from the internal circuit, the clock signal output by the clock receiver clocking the parallel-to-serial shift register.

8 (Currently Amended). The device of claim 7 wherein the slave circuit further includes a logic circuit connected to the first multiplexor, the second multiplexor, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

9 (Currently Amended). The device of claim 8 wherein the media receiver receives a signal from the transmission media having a first frequency, wherein ~~the~~ a signal output from the serdes has a second frequency, and wherein the first frequency and the second frequency are substantially equivalent.

10 (Currently Amended). A processing circuit comprising:

~~an internal circuit; and~~

~~a slave circuit connected to the internal circuit, the slave circuit having:~~

———a clock receiver connectable to a clock driver, the clock receiver outputting a clock signal in response to a first differential signal received from the clock driver;

———a first processing data receiver connectable to the first physical layer data driver, the first processing data receiver outputting a first signal in response to a second differential signal received from the first physical layer data driver; and

———a first processing data driver connectable to a first physical layer data receiver, the first processing data driver being connectable to receive the clock signal from the clock receiver or the first signal from the first processing data receiver.

11 (Currently Amended). The circuit of claim 10 wherein the ~~slave~~ processing circuit further comprises:

a first multiplexer connected to the clock ~~input~~ receiver and the first processing data receiver, the first multiplexer passing the clock signal output by the clock receiver when a first mux signal is in a first logic state, and passing the first signal output by the first processing data receiver when the first mux signal is in a second logic state; and

a second multiplexer connected to the first multiplexer and

the first ~~communication~~ processing data driver, the second multiplexer passing a signal output from the first multiplexer when a second mux signal is in a first logic state, and passing an output data signal when the second mux signal is in a second logic state, the signal output from the first multiplexer being the clock signal when the first mux signal is in the first logic state, and being the first signal when the first mux signal is in the second logic state.

12 (Currently Amended). The circuit of claim 11 wherein the ~~slave~~ processing circuit further comprises a serial-to-parallel shift register ~~connected to the internal circuit~~, the clock receiver, and the first processing data receiver, the clock signal output by the clock receiver clocking the serial-to-parallel shift register.

13 (Currently Amended). The circuit of claim 12 wherein the ~~slave~~ processing circuit further comprises a parallel-to-serial shift register ~~connected to the internal circuit~~, the second multiplexer, and the clock receiver, the parallel-to-serial shift register outputting a data output signal in response to a parallel data signal ~~from the internal circuit~~, the clock signal output by the receiver clocking the parallel-to-serial shift

register.

14 (Currently Amended). The circuit of claim 13 wherein the ~~slave~~ processing circuit further ~~includes~~ comprises a logic circuit connected to the first multiplexor, the second multiplexor, and the parallel-to-serial shift register, the logic circuit receiving the clock signal from the parallel-to-serial shift register, and setting the logic states of the first and second mux signals in response to commands extracted from the clock signal.

15 (Currently Amended). A physical layer device connectable to a transmission medium, the device comprising:

~~a media driver connectable to the transmission medium;~~

a media receiver connectable to the transmission medium;

a serializer/deserializer (serdes) connected to the ~~media driver and the~~ media receiver, the serdes outputting a master clock signal, an equivalent in-phase slave clock signal when in a calibration mode, and a data signal when in a data mode, the data signal representing a data signal received from the media receiver; and

a master circuit, the master circuit having:

a clock driver connected to output the master clock

signal as a first differential signal; and

a first physical layer data driver connectable to output the slave clock signal as a second differential signal when the serdes is in the calibration mode, and the data signal as a third differential signal when the serdes is in the data mode.

16 (Original). The device of claim 15 wherein the master circuit further includes:

a first physical layer data receiver that receives a signal which represents the master clock signal during a first phase of the calibration mode, and represents the slave clock signal during a second phase of the calibration mode; and

an aligner connected to the first physical layer data receiver, the aligner receiving the master clock signal when the first physical layer data receiver receives the master clock signal, and the slave clock signal when the first physical layer data receiver receives the slave clock signal, the aligner having phase comparison circuitry that compares a phase of the master clock signal received by the aligner with a phase of the slave clock signal received by the aligner to determine a phase difference.

17 (Original). The device of claim 16 wherein the master circuit further comprises a phase delay circuit connected to the aligner, the serdes, and the first physical layer data driver, the aligner passing a plurality of signals to the phase delay circuit that indicates the phase difference, the phase delay circuit delaying the slave clock signal output from the serdes an amount so that the slave clock signal received by the aligner is substantially in phase with the master clock signal received by the aligner when in the calibration mode, the data signal being delayed the amount when in the data mode.

18 (Previously Presented). A method for operating a communication device having a physical layer device connected to a transmission medium and a processing device connected to the physical layer device, the method comprising the steps of:

outputting a master clock signal from the physical layer device over a first path;

receiving the master clock signal in the processing device from the first path;

outputting the master clock signal as a feedback master clock signal from the processing device over a feedback path;

receiving the feedback master clock signal in the physical layer device from the feedback path;

determining a phase of the feedback master clock signal;

outputting a slave clock signal from the physical layer device over a second path after the phase of the feedback master clock signal has been determined;

receiving the slave clock signal in the processing device from the second path;

outputting the slave clock signal as a feedback slave clock signal from the processing device over the feedback path;

receiving the feedback slave clock signal in the physical layer device from the feedback path;

determining a phase of the feedback slave clock signal;

comparing the phase of the feedback master clock signal with the phase of the feedback slave clock signal to determine a phase difference; and

adjusting a delay so that the phase of the feedback slave clock signal is substantially aligned with the phase of the feedback master clock signal.

19 (Original). The method of claim 18 and further comprising the steps of:

outputting a data clock signal from the physical layer device over the first path after the phase difference has been determined;

outputting an input data signal from the physical layer device over the second path after the phase difference has been determined, the input data signal and data clock signal having an equivalent frequency; and

converting the input data signal to a parallel word by clocking the input data signal with the data clock signal.

20 (Previously Presented). A communication device comprising:

a physical layer device connectable to a transmission medium, the device having a master circuit, the master circuit having:

a clock output;

a first data output;

a first data input; and

a phase comparator connected to the first data input; and

a processing circuit having a slave circuit, the slave circuit having:

a clock input connected to the clock output;

a second data input connected to the first data output;

a second data output connected to the first data input; and

a switch for connecting an output signal from the clock input to the second data output, or an output signal from the second data input to the second data output, the phase comparator comparing a phase of the output signal from the clock input with a phase of the output signal from the second data input to determine a phase difference.